# ILI211XA

# FW Update Programming Guide



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*Document Revision History*

| Version | Data | Author | Description |
|---|---|---|---|
| 1.0.0.0 | 2018/10/22 | Vincent Chen | First Release Version |
| 2.0.0.0 | 2019/1/31 | Max | |
| 3.0.0.0 | 2019/3/6 | Luca Hsu | Add Memory Map |

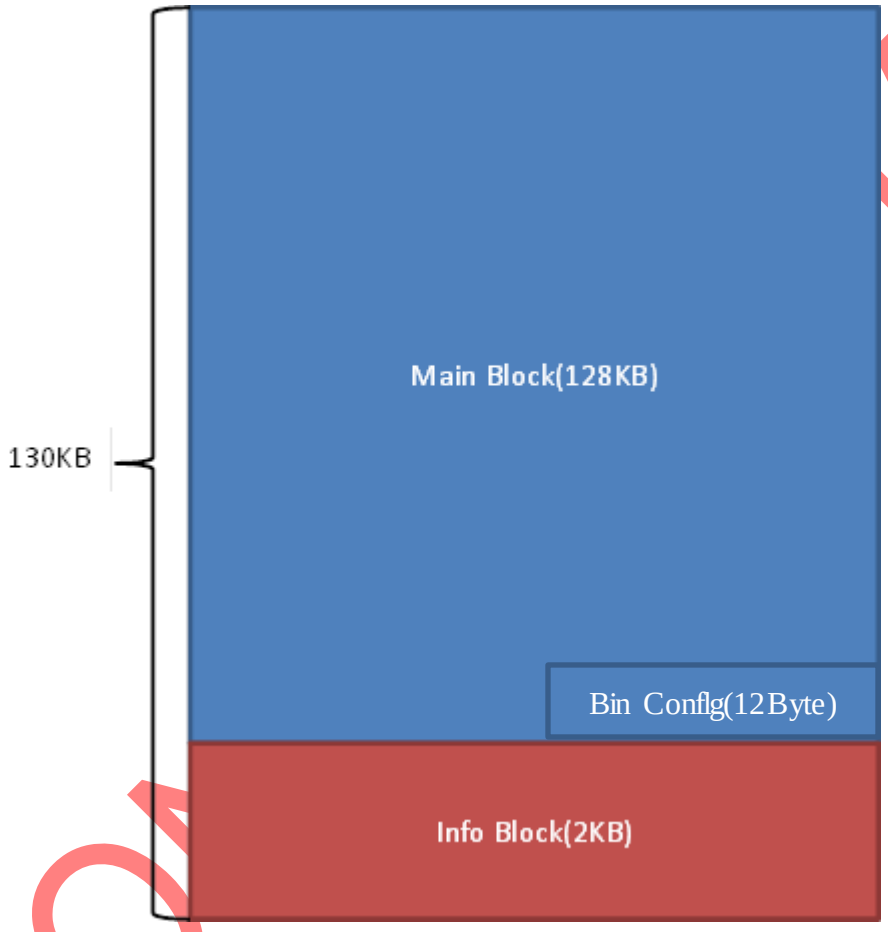
## TABLE OF CONTENTS

# 1. Introduction

## 1. Overview

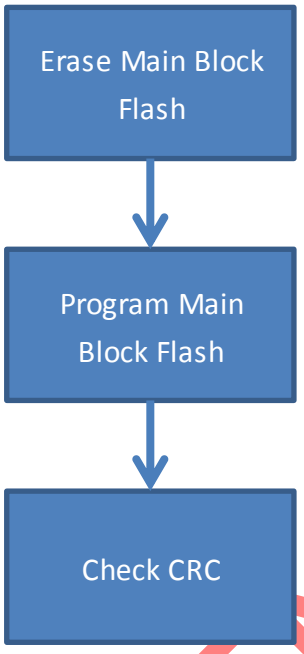
This document defines a guide of ILITEK ILI2117A, ILI2118A FW update. Supported interface has I2C only. FW update can be done by Ilitek MP Tool, TP Test Studio as well with windows OS.

## 2. Memory Map



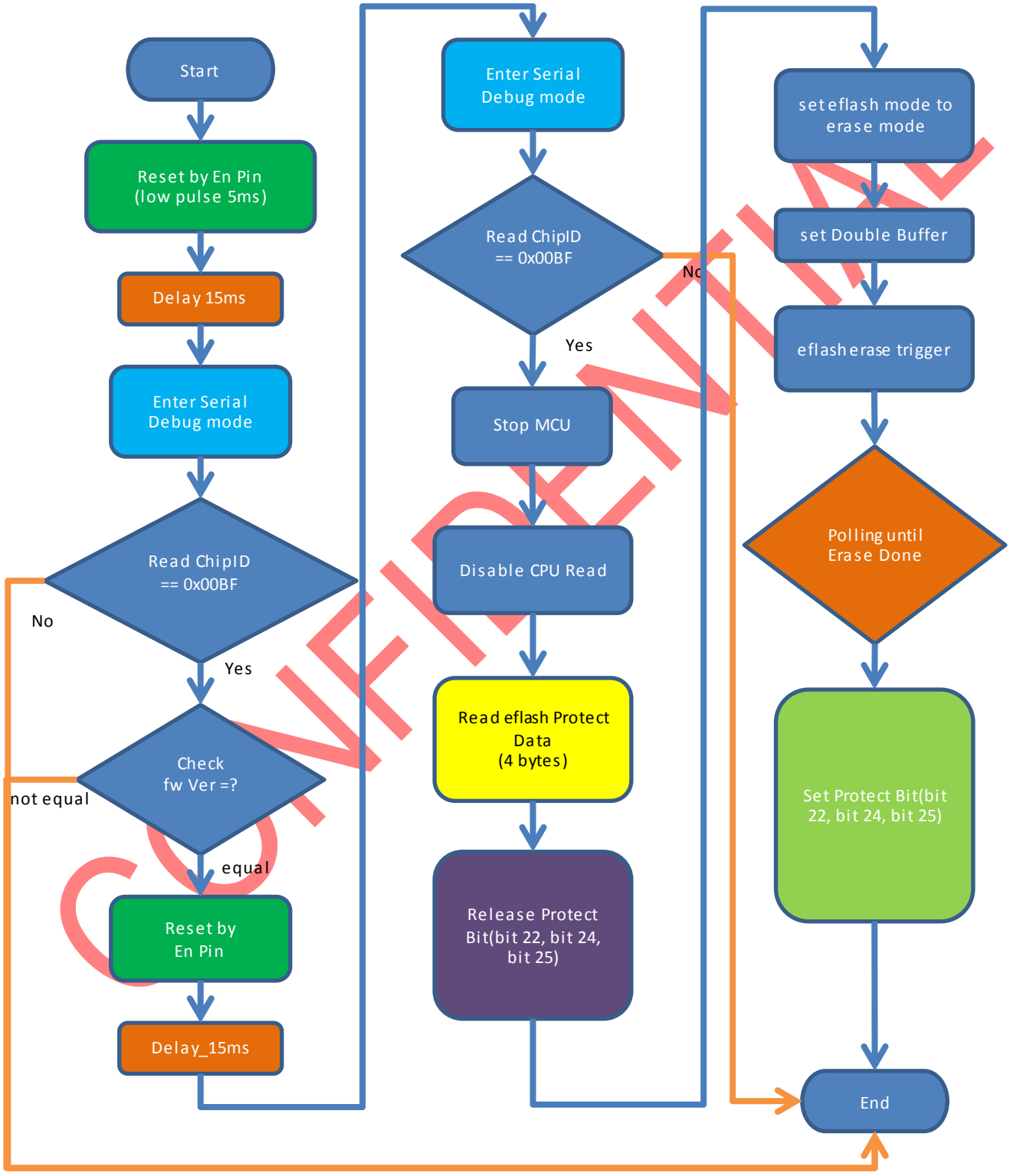

| Bin Config | | | | | |
|---|---|---|---|---|---|
| 0x1FFF4 | 0x1FFF5 | 0x1FFF6 | 0x1FFF7 | 0x1FFF8 | 0x1FFF9 |
| Major(LSB) | Major(MSB) | Minor(LSB) | Minor(MSB) | Reserved | Reserved |
| 0x1FFFA | 0x1FFFB | 0x2FFFC | 0x3FFFD | 0x4FFFE | 0x5FFFF |
| Reserved | Reserved | CRC32(LSB) | CRC32 | CRC32 | CRC32(MSB) |

## 3. FW Update Flow Chart



# 2. Detail of each function

## 1. Flash Erase Flow Chart



➢ **Detail of Flash Erase**

Note : [release protect bit] – index 63~65, set bit 22, bit 24, bit 25 to 0;
[set protect bit] – index 91~94, recover bit 22, bit 24, bit 25 to 1.

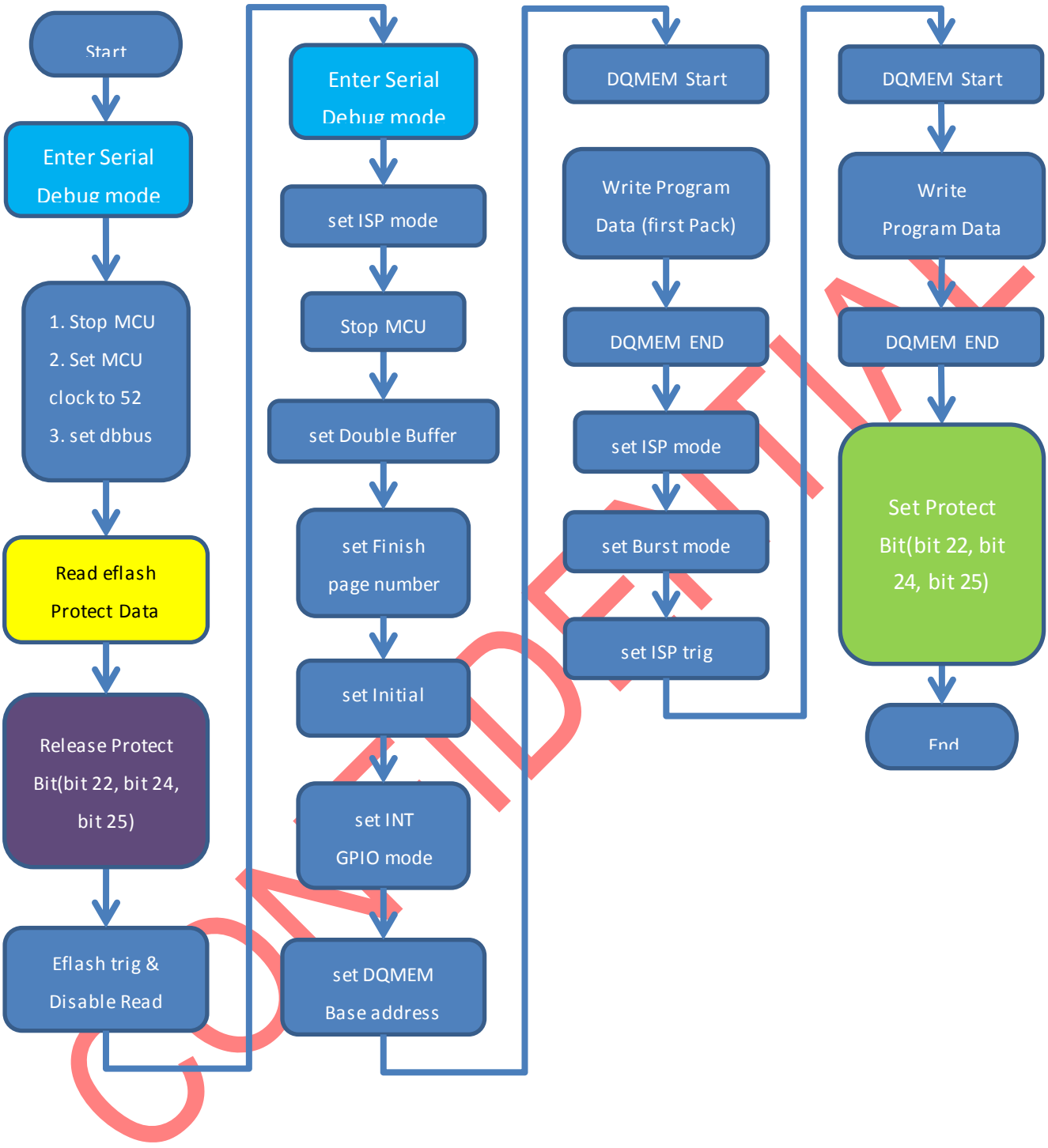
| Comment | Index | Addr | Phase | Data | | | | |
|---|---|---|---|---|---|---|---|---|
| Reset EN Pin(Low pulse 5ms) | | | | | | | | |
| Delay 15ms | | | | | | | | |
| Enter Serial Debug Mode | 1 | 62 | Write | 53 | 45 | 52 | 44 | 42 |
| | 2 | 62 | Write | 37 | | | | |
| | 3 | 62 | Write | 61 | | | | |
| | 4 | 62 | Write | 35 | | | | |
| | 5 | 62 | Write | 71 | | | | |
| | 6 | 62 | Write | 80 | | | | |
| | 7 | 62 | Write | 82 | | | | |
| | 8 | 62 | Write | 84 | | | | |
| | 9 | 62 | Write | 10 | 1E | 8 | | |
| | 10 | 62 | Read | 0 | 80 | | | |
| | 11 | 62 | Write | 10 | 1E | 8 | 0 | 0 |
| | 12 | 62 | Write | 10 | 1E | 9E | | |
| | 13 | 62 | Read | 0 | 80 | | | |
| | 14 | 62 | Write | 10 | 1E | 9E | 0 | 80 |
| Read CHIP ID | 15 | 62 | Write | 10 | 1E | CC | | |
| CHIP ID must equal to 0x00BF | 16 | 62 | Read | BF | 0 | | | |
| Disable Watch Dog | 17 | 62 | Write | 10 | 3C | 60 | 55 | |
| | 18 | 62 | Write | 10 | 3C | 61 | AA | |
| Check FW Ver. & I2C ID | 19 | 62 | Write | 10 | 3A | 8 | | |
| | 20 | 62 | Read | 26 | 0 | | | |
| | 21 | 62 | Write | 10 | 17 | 0A | 4 | |
| | 22 | 62 | Read | 0 | 0 | | | |
| | 23 | 62 | Write | 10 | 0F | E6 | 1 | 0 |
| | 24 | 62 | Write | 10 | 0F | E6 | 0 | 0 |
| | 25 | 26 | Write | 3 | | | | |
| | 26 | 26 | Read | Version0 | Version1 | Version2 | Version3 | |
| | 27 | 62 | Write | 10 | 0F | E6 | 0 | 0 |
| Reset EN Pin(Low pulse 5ms) | | | | | | | | |
| Delay 15ms | | | | | | | | |
| Enter Serial Debug Mode | 28 | 62 | Write | 53 | 45 | 52 | 44 | 42 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 29 | 62 | Write | 37 | | | | |
| | 30 | 62 | Write | 61 | | | | |
| | 31 | 62 | Write | 35 | | | | |
| | 32 | 62 | Write | 71 | | | | |
| | 33 | 62 | Write | 80 | | | | |
| | 34 | 62 | Write | 82 | | | | |
| | 35 | 62 | Write | 84 | | | | |
| | 36 | 62 | Write | 10 | 1E | 8 | | |
| | 37 | 62 | Read | 0 | 80 | | | |
| | 38 | 62 | Write | 10 | 1E | 8 | 0 | 0 |
| | 39 | 62 | Write | 10 | 1E | 9E | | |
| | 40 | 62 | Read | 0 | 80 | | | |
| | 41 | 62 | Write | 10 | 1E | 9E | 0 | 80 |
| Read CHIP ID | 42 | 62 | Write | 10 | 1E | CC | | |
| | 43 | 62 | Read | BF | 0 | | | |
| Disable Watch Dog | 17 | 62 | Write | 10 | 3C | 60 | 55 | |
| | 18 | 62 | Write | 10 | 3C | 61 | AA | |
| Stop MCU | 44 | 62 | Write | 10 | 0F | E6 | 1 | 0 |
| Disable CPU Read | 45 | 62 | Write | 10 | 16 | 8 | 20 | |
| | 46 | 62 | Write | 10 | 16 | 6 | 20 | |
| Set eflash mode | 47 | 62 | Write | 10 | 16 | 6 | 1 | |
| to read mode | 48 | 62 | Write | 10 | 16 | 10 | 1 | |
| | 49 | 62 | Write | 10 | 16 | 7 | 20 | |
| Set read address | 50 | 62 | Write | 10 | 16 | 0 | 3 | |
| | 51 | 62 | Write | 10 | 16 | 1 | 0 | |
| Read Protect Data | 52 | 62 | Write | 10 | 16 | 0A | | |
| SFR_ADDR3_BYTE0_1_VALUE | 53 | 62 | Read | Bit[0:7] | Bit[8:15] | | | |
| Read Protect Data | 54 | 62 | Write | 10 | 16 | 0C | | |
| SFR_ADDR3_BYTE2_3_VALUE | 55 | 62 | Read | Bit[16:23] | Bit[24:31] | | | |
| Disable Read CPU Read | 56 | 62 | Write | 10 | 16 | 8 | 20 | |
| | 57 | 62 | Write | 10 | 16 | 6 | 20 | |
| Set eflash test mode | 58 | 62 | Write | 10 | 16 | 10 | 80 | |
| | 59 | 62 | Write | 10 | 16 | 7 | 10 | |
| Set Double Buffer | 60 | 62 | Write | 10 | 16 | 4 | 1 | |
| Trig SFR Write | 61 | 62 | Write | 10 | 16 | 6 | 1 | |
| write Protect data, Bit [0:7] | 62 | 62 | Write | 10 | 16 | 2 | Bit [0:7] | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| write Protect data, Bit [8:15] | 63 | 62 | Write | 10 | 16 | 2 | Bit [8:15] | |
| write Protect data, Bit [16:23], set bit 22 to 0. | 64 | 62 | Write | 10 | 16 | 2 | Bit [16:23] | |
| write Protect data, Bit [24:31], set bit 24, bit 25 to 0. | 65 | 62 | Write | 10 | 16 | 2 | Bit [24:31] | |
| Set write address | 66 | 62 | Write | 10 | 16 | 0 | 3 | |
| | 67 | 62 | Write | 10 | 16 | 1 | 0 | |
| Set TM mode = 0 | 68 | 62 | Write | 10 | 16 | 7 | 0 | |
| Set double buffer | 69 | 62 | Write | 10 | 16 | 4 | 1 | |
| Eflash trig & disable | 70 | 62 | Write | 10 | 16 | 6 | 1 | |
| Read function | 71 | 62 | Write | 10 | 16 | 6 | 20 | |
| Set Program/Erase password | 72 | 62 | Write | 10 | 16 | 18 | A5 | 5A |
| Set eFlash mode to erase mode | 73 | 62 | Write | 10 | 16 | 6 | C0 | |
| Mass Erase | 74 | 62 | Write | 10 | 16 | 7 | 3 | |
| Set Double Buffer | 75 | 62 | Write | 10 | 16 | 4 | 1 | |
| Eflash mode trigger | 76 | 62 | Write | 10 | 16 | 6 | C1 | |
| **Polling** read 0x160E | 77 | 62 | Write | 10 | 16 | 0E | | |
| Until reg[bit3] =1 | 78 | 62 | Read | 1 | | | | |
| | 79 | 62 | Write | 10 | 16 | 0E | | |
| | 80 | 62 | Read | 9 | | | | |
| Clear eflash setting | 81 | 62 | Write | 10 | 16 | 6 | 0 | |
| | 82 | 62 | Write | 10 | 16 | 7 | 0 | |
| Set Double Buffer | 83 | 62 | Write | 10 | 16 | 4 | 1 | |
| Clear Program/Erase | 84 | 62 | Write | 10 | 16 | 18 | 5A | A5 |
| Password | 85 | 62 | | | | | | |
| Disable Read CPU Read | 86 | 62 | Write | 10 | 16 | 8 | 20 | |
| | 87 | 62 | Write | 10 | 16 | 6 | 20 | |
| | 88 | 62 | Write | 10 | 16 | 10 | 80 | |
| Set eflash test mode | 89 | 62 | Write | 10 | 16 | 7 | 10 | |
| Set Double Buffer | 90 | 62 | Write | 10 | 16 | 4 | 1 | |
| Trig SFR write | 91 | 62 | Write | 10 | 16 | 6 | 1 | |
| write Protect data, Bit [0:7] | 92 | 62 | Write | 10 | 16 | 2 | Bit [0:7] | |
| write Protect data, Bit [8:15] | 93 | 62 | Write | 10 | 16 | 2 | Bit [8:15] | |
| write Protect data, Bit [16:23], recover bit 22 to 1 | 94 | 62 | Write | 10 | 16 | 2 | Bit [16:23] | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| write Protect data,<br>Bit [24:31], recover bit 24, bit 25 to 1 | 95 | 62 | Write | 10 | 16 | 2 | Bit [24:31] | |
| Set write address | 96 | 62 | Write | 10 | 16 | 0 | 3 | |
| | 97 | 62 | Write | 10 | 16 | 1 | 0 | |
| | 98 | 62 | Write | 10 | 16 | 6 | 2 | |

## 2. Program Data Flow Chart– Main Block



➢ **Detail of Program Main Block**

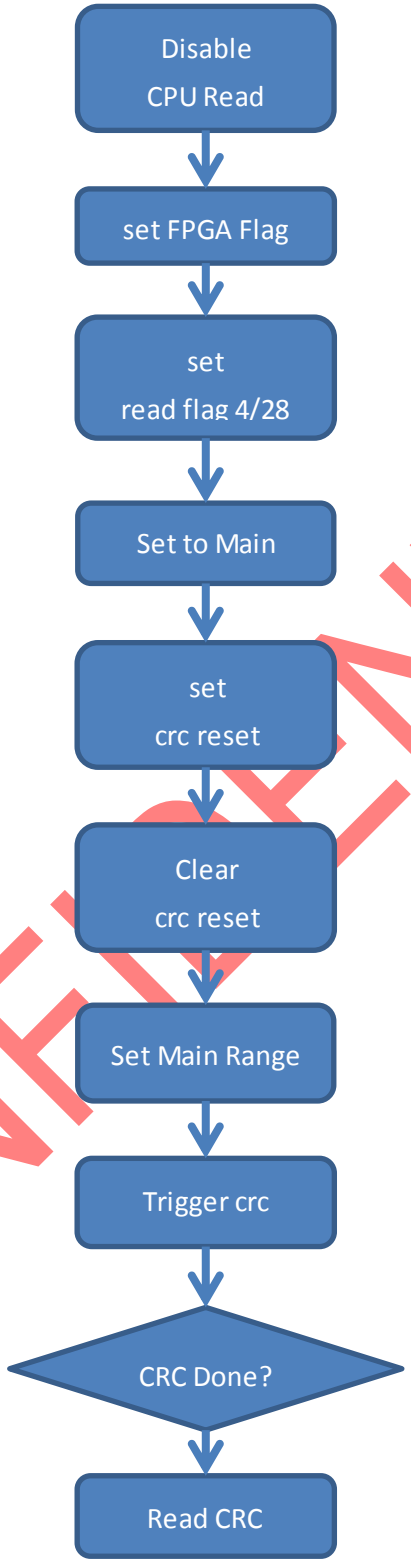
| Comment | Index | Addr | Phase | Data | | | | |
|---|---|---|---|---|---|---|---|---|
| Enter Serial Debug Mode | 1 | 62 | Write | 53 | 45 | 52 | 44 | 42 |
| | 2 | 62 | Write | 37 | | | | |
| | 3 | 62 | Write | 61 | | | | |
| | 4 | 62 | Write | 35 | | | | |
| | 5 | 62 | Write | 71 | | | | |
| | 6 | 62 | Write | 80 | | | | |
| | 7 | 62 | Write | 82 | | | | |
| | 8 | 62 | Write | 84 | | | | |
| | 9 | 62 | Write | 10 | 1E | 8 | | |
| | 10 | 62 | Read | 0 | 80 | | | |
| | 11 | 62 | Write | 10 | 1E | 8 | 0 | 0 |
| | 12 | 62 | Write | 10 | 1E | 9E | | |
| | 13 | 62 | Read | 0 | 80 | | | |
| | 14 | 62 | Write | 10 | 1E | 9E | 0 | 80 |
| Read CHIP ID | 15 | 62 | Write | 10 | 1E | CC | | |
| CHIP ID must equal to 0x00BF | 16 | 62 | Read | BF | 0 | | | |
| Disable Watch Dog | 17 | 62 | Write | 10 | 3C | 60 | 55 | |
| | 18 | 62 | Write | 10 | 3C | 61 | AA | |
| Stop MCU | 19 | 62 | Write | 10 | 0F | E6 | 1 | |
| set MCU clock to 52 | 20 | 62 | Write | 10 | 1E | 22 | 0 | C0 |
| set dbbus speed to /1 | 21 | 62 | Write | 10 | 1E | 24 | 0 | 0 |
| Set Program/Erase password | 22 | 62 | Write | 10 | 16 | 18 | A5 | 5A |
| Disable Read CPU Read | 23 | 62 | Write | 10 | 16 | 8 | 20 | |
| | 24 | 62 | Write | 10 | 16 | 6 | 20 | |
| Set eflash mode to read mode | 25 | 62 | Write | 10 | 16 | 6 | 1 | |
| | 26 | 62 | Write | 10 | 16 | 10 | 1 | |
| | 27 | 62 | Write | 10 | 16 | 7 | 20 | |
| set double buffer | 28 | 62 | Write | 10 | 16 | 4 | 1 | |
| Set read address | 29 | 62 | Write | 10 | 16 | 0 | 3 | |
| | 30 | 62 | Write | 10 | 16 | 1 | 0 | |
| Read Protect Data | 31 | 62 | Write | 10 | 16 | 0A | | |
| SFR_ADDR3_BYTE0_1_VALUE | 32 | 62 | Read | Bit[0:7] | Bit[8:15] | | | |
| Read Protect Data | 33 | 62 | Write | 10 | 16 | 0C | | |
| SFR_ADDR3_BYTE2_3_VALUE | 34 | 62 | Read | Bit[16:23] | Bit[24:31] | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Disable Read CPU Read | 35 | 62 | Write | 10 | 16 | 8 | 20 | |
| | 36 | 62 | Write | 10 | 16 | 6 | 20 | |
| Set eflash test mode | 37 | 62 | Write | 10 | 16 | 10 | 80 | |
| | 38 | 62 | Write | 10 | 16 | 7 | 10 | |
| Set Double Buffer | 39 | 62 | Write | 10 | 16 | 4 | 1 | |
| Trig SFR Write | 40 | 62 | Write | 10 | 16 | 6 | 1 | |
| write Protect data, Bit [0:7] | 41 | 62 | Write | 10 | 16 | 2 | Bit[0:7] | |
| write Protect data, Bit [8:15] | 42 | 62 | Write | 10 | 16 | 2 | Bit[8:15] | |
| write Protect data, Bit [16:23], set bit 22 to 0. | 43 | 62 | Write | 10 | 16 | 2 | Bit[16:23] | |
| write Protect data, Bit [24:31], set bit 24, bit 25 to 0. | 44 | 62 | Write | 10 | 16 | 2 | Bit[24:31] | |
| Set write address | 45 | 62 | Write | 10 | 16 | 0 | 3 | |
| | 46 | 62 | Write | 10 | 16 | 1 | 0 | |
| Set TM mode = 0 | 47 | 62 | Write | 10 | 16 | 7 | 0 | |
| Set double buffer | 48 | 62 | Write | 10 | 16 | 4 | 1 | |
| Eflash trig & disable | 49 | 62 | Write | 10 | 16 | 6 | 1 | |
| Read function | 50 | 62 | Write | 10 | 16 | 6 | 20 | |
| Enter Serial Debug Mode | 51 | 62 | Write | 53 | 45 | 52 | 44 | |
| | 52 | 62 | Write | 37 | | | | |
| | 53 | 62 | Write | 61 | | | | |
| | 54 | 62 | Write | 35 | | | | |
| | 55 | 62 | Write | 71 | | | | |
| Set isp mode reg 0x1EBE[bit15], set "1" | 56 | 62 | Write | 10 | 1E | BE | | |
| | 57 | 62 | Read | 2 | 0 | | | |
| | 58 | 62 | Write | 10 | 1E | BE | 2 | |
| | 59 | 62 | Write | 10 | 1E | BF | 80 | |
| Set Program/Erase password | 60 | 62 | Write | 10 | 16 | 18 | A5 | |
| | 61 | 62 | Write | 10 | 16 | 19 | 5A | |
| Stop MCU | 62 | 62 | Write | 10 | 0F | E6 | 1 | |
| | 63 | 62 | Write | 10 | 0F | E7 | 0 | |
| Set Double Buffer | 64 | 62 | Write | 10 | 16 | 4 | 1 | |
| Set finish page number | 65 | 62 | Write | 10 | 16 | 1A | 0 | |
| page number = 0x0000 | 66 | 62 | Write | 10 | 16 | 1B | 0 | |
| Set Initial Address | 67 | 62 | Write | 10 | 16 | 0 | 0 | |
| Address = 0x0000 | 68 | 62 | Write | 10 | 16 | 1 | 0 | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| set INT GPIO mode | 69 | 62 | Write | 10 | 3C | 0 | | |
| | 70 | 62 | Read | 88 | | | | |
| | 71 | 62 | Write | 10 | 3C | 0 | 89 | |
| | 72 | 62 | Write | 10 | 3C | 1 | 0 | |
| | | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| Set DQMEM base address | 77 | 62 | Write | 10 | 1E | 34 | 0 | |
| DQMEM base address = 0x0000 | 78 | 62 | Write | 10 | 1E | 35 | 0 | |
| DQMEM Start | 79 | 62 | Write | 7F | | | | |
| | 80 | 62 | Write | 50 | | | | |
| | 81 | 62 | Write | 51 | | | | |
| | 82 | 62 | Write | 54 | | | | |
| | 83 | 62 | Write | 80 | | | | |
| | 84 | 62 | Write | 82 | | | | |
| | 85 | 62 | Write | 85 | | | | |
| | 86 | 62 | Write | 35 | | | | |
| Write Program Data (first Pack:0x00~0x0100) | 87 | 62 | Write | **10** | **0** | **0** | 00(256Byte) | |
| DQMEM END | 88 | 62 | Write | 7E | | | | |
| Set isp mode reg 0x1EBE[bit15], set "1" | 73 | 62 | Write | 10 | 1E | BE | | |
| | 74 | 62 | Read | 2 | 80 | | | |
| | 75 | 62 | Write | 10 | 1E | BE | 2 | |
| | 76 | 62 | Write | 10 | 1E | BF | 80 | |
| set Burst mode | 77 | 62 | Write | 10 | 16 | 8 | | |
| | 78 | 62 | Read | 20 | 0 | | | |
| | 79 | 62 | Write | 10 | 16 | 8 | 21 | |
| set isp trig | 80 | 62 | Write | 10 | 16 | 1A | | |
| | 81 | 62 | Read | 0 | 0 | | | |
| | 82 | 62 | Write | 10 | 1E | 1A | 0 | |
| | 83 | 62 | Write | 10 | 1E | 1B | 20 | |
| DQMEM Start | 84 | 62 | Write | 7F | | | | |
| | 85 | 62 | Write | 50 | | | | |
| | 86 | 62 | Write | 51 | | | | |
| | 87 | 62 | Write | 54 | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 88 | 62 | Write | 80 | | | | |
| | 89 | 62 | Write | 82 | | | | |
| | 89 | 62 | Write | 85 | | | | |
| | 90 | 62 | Write | 35 | | | | |
| Write Program Data (Bin file 0x0100~0x01FFFF) | 91 | 62 | Write | **10** | **0** | **0** | 90 | F2 |
| Disable Read CPU Read | 92 | 62 | Write | 10 | 16 | 8 | 20 | |
| | 93 | 62 | Write | 10 | 16 | 6 | 20 | |
| Set eflash test mode | 94 | 62 | Write | 10 | 16 | 10 | 80 | |
| | 95 | 62 | Write | 10 | 16 | 7 | 10 | |
| Set Double Buffer | 96 | 62 | Write | 10 | 16 | 4 | 1 | |
| Trig wfr write | 97 | 62 | Write | 10 | 16 | 6 | 1 | |
| write Protect data, Bit [0:7] | 98 | 62 | Write | 10 | 16 | 2 | Bit[0:7] | |
| write Protect data, Bit [8:15] | 99 | 62 | Write | 10 | 16 | 2 | Bit[8:15] | |
| write Protect data, Bit [16:23], recover bit 22 to 1 | 100 | 62 | Write | 10 | 16 | 2 | Bit[16:23] | |
| write Protect data, Bit [24:31], recover bit 24, bit 25 to 1 | 101 | 62 | Write | 10 | 16 | 2 | Bit[24:31] | |
| Set write address | 102 | 62 | Write | 10 | 16 | 0 | 3 | |
| | 103 | 62 | Write | 10 | 16 | 1 | 0 | |
| | 104 | 62 | Write | 10 | 16 | 6 | 2 | |

## 3. CRC Flow Chart



➢ **Detail of CRC Flow**

| Comment | Index | Addr | Phase | Data | | | | |
|---|---|---|---|---|---|---|---|---|
| Disable CPU read | 1 | 62 | Write | 10 | 16 | 08 | 20 | |
| | 2 | 62 | Write | 10 | 16 | 06 | 20 | |
| Set FPGA Flag | 3 | 62 | Write | 10 | 16 | 10 | 00 | |
| Set read flag 4/28 | 4 | 62 | Write | 10 | 16 | 10 | 01 | |
| Set Block | 5 | 62 | Write | 10 | 16 | 06 | 00 | |
| | 6 | 62 | Write | 10 | 16 | 04 | 01 | |
| Set CRC reset | 7 | 62 | Write | 10 | 16 | 20 | 02 | |
| Clr CRC reset | 8 | 62 | Write | 10 | 16 | 20 | 00 | |
| Set Range | 9 | 62 | Write | 10 | 16 | 00 | 00 | 00 |
| | 10 | 62 | Write | 10 | 16 | 22 | FF | 07 |
| Trig crc | 11 | 62 | Write | 10 | 16 | 20 | 01 | |
| Polling CRC result [bit15] = 0? | 12 | 62 | Write | 10 | 16 | 20 | | |
| | 13 | 62 | Read | 00 | 80 | | | |
| | 15 | 62 | Write | 10 | 16 | 20 | | |
| | 16 | 62 | Read | 00 | 00 | | | |
| Read CRC Result | 18 | 62 | Write | 10 | 16 | 26 | | |
| | 19 | 62 | Read | High | CRC | | | |
| | 20 | 62 | Write | 10 | 16 | 24 | | |
| | 22 | 62 | Read | Low | CRC | | | |
| Reset EN Pin(Low pulse 5ms) | | | | | | | | |
| Delay 15ms | | | | | | | | |